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EXAMINER	
LI, AIMEE J	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
06/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/015,530	PLUNKETT ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/6/08; 12/19/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been considered. Claims 1, 6, 11, 16, 19, and 21 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as filed 19 December 2008; Terminal Disclaimer for 6,836,839 as filed 09 March 2009; Terminal Disclaimer for 6,986,021 as filed 09 March 2009; and Amendment as filed 09 March 2009.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings contain handwritten and hand-drawn elements and other informalities as indicated in the Notice of Draftperson's Patent Drawing Review dated 12 July 2004. The Notice was mailed with the Non-Final Office Action dated 14 July 2004, but no formal drawings were filed. As such, the drawings still remain objected to, as indicated in the Notice of Draftperson's Patent Drawing Review. A copy of the original Notice is accompanying this office action.

4. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 06 June 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner. In light of arguments presented, the Examiner has considered the references cited in this IDS. However, it is desirable to avoid the submission of long lists of documents if it can be avoided. Clearly irrelevant and marginally pertinent cumulative information should be eliminated. If a long list is submitted, those documents which have been specifically brought to applicant's attention and/or are known to be of most significance should be highlighted. See Penn Yan Boats, Inc. v. Sea Lark Boats, Inc., 359 F. Supp. 948, 175 USPQ 260 (S.D. Fla. 1972), aff'd, 479 F.2d 1338, 178 USPQ 577 (5th Cir. 1973), cert. denied, 414 U.S. 874 (1974). But cf. Molins PLC v. Textron Inc., 48 F.3d 1172, 33 USPQ2d 1823 (Fed. Cir. 1995). See MPEP 2004.

6. Applicant's duty of disclosure of material and information is not satisfied by presenting a patent examiner with "a mountain of largely irrelevant [material] from which he is presumed to have been able, with his expertise and with adequate time, to have found the critical [material]. It ignores the real world conditions under which examiners work." Rohm & Haas Co. v. Crystal Chemical Co., 722 F.2d 1556, 1573 [220 USPQ 289] (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). (Emphasis in original). Applicant has a duty not just to disclose pertinent prior art references but to make a disclosure in such way as not to "bury" it within other disclosures of less relevant prior art; See Golden Valley Microwave Foods Inc. v. Weaver Popcorn Co. Inc., 24 USPQ2d 1801 (N.D. Ind. 1992); Molins PLC v. Textron Inc., 26 USPQ2d 1889, at 1899 (D.Del 1992); Penn Yan Boats, Inc. v. Sea Lark Boats, Inc. et al., 175 USPQ 260, at 272 (S.D. Fl. 1972).

7. The examiner is not afforded the time to thoroughly review each reference, given the number of references cited. By initialing each of the cited references on the accompanying 1449 form(s), the examiner is merely acknowledging the submission of the cited references and indicating that only a cursory review was made of the cited references.

8. The information disclosure statement filed 19 December 2008 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because some of the prior art listed have been previously listed in the now considered IDS filed 06 June 2008. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Response to Arguments

9. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 21 and 23-25 are rejected under 35 U.S.C. 102(b) as being taught by Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove).

12. Referring to claim 21, Gove has taught a method for allocating hardware resources within an adaptive computing integrated circuit, comprising:

a. in response to first configuration information, configuring a first group of heterogeneous computational elements to form a first functional unit to implement a first function and configuring a second group of heterogeneous computational elements to form a second functional unit to implement a second function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64); and

b. in response to second configuration information, reconfiguring one or more of the second group of heterogeneous computational elements to implement the first function while the first functional unit is implements the first function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

13. Referring to claim 23, Gove has taught the method of claim 21 wherein in response to the second configuration information, the one or more of the second group of heterogeneous computational elements are reconfigured to form one or more additional instances of the first

functional unit to implement the first function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

14. Referring to claim 24, Gove has taught the method of claim 21 wherein in response to the second configuration information, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigured to form a single functional unit to implement the first function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

15. Referring to claim 25, Gove has taught the method of claim 21 further comprising: in response to third configuration information, reconfiguring one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements to implement a third function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove) as applied to claim 21 above, and further in view of Hung et al., U.S. Patent Number 6,526,430 (herein referred to as Hung).

18. Gove has not taught the method of claim 21 wherein the second configuration information is generated when the second function is not currently used. Hung has taught reconfiguring multiple computation elements to function on different functions based upon need and availability (Hung column 9, line 5 to column 10, line 5). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hung in the device of Gove to reduce idle time of computation elements and minimize mode switching, thereby increasing the overall efficiency of the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the reconfiguring of Hung in the device of Gove to improve overall efficiency of the system.

19. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove) in view of Hung et al., U.S. Patent Number 6,526,430 (herein referred to as Hung).

20. Referring to claim 1, Gove has taught an adaptive computing integrated circuit configurable to perform a plurality of functions, comprising:

a. a first computational unit including a first plurality of heterogeneous computational elements (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column

26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64) and

b. a first computational interconnection network coupled to the plurality of heterogeneous computational elements, the first computational interconnection network operative to configure connections between the first plurality of heterogeneous computational elements (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

c. a second digital processing unit including a second plurality of heterogeneous computational elements and a digital processing computational interconnection network coupled to the second plurality of heterogeneous computational elements, the second computational interconnection network operative to configure the connections between the second plurality of heterogeneous elements (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

d. wherein a first group of the first and second plurality of heterogeneous computational elements is configurable to form a first functional unit to implement a first function (Gove column 9, line 27 to column 10, line 4; Figure

10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

e. wherein a second group of the first and second plurality of heterogeneous computational elements is configurable to form a second functional unit to implement a second function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64); and

f. wherein one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection networks to implement the first function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

21. Gove has not taught reconfiguring the computational elements if the second function is not currently used. Hung has taught reconfiguring multiple computation elements to function on different functions based upon need and availability (Hung column 9, line 5 to column 10, line 5). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hung in the device of Gove to reduce idle time of computation elements and minimize mode switching, thereby increasing the overall efficiency of the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to incorporate the reconfiguring of Hung in the device of Gove to improve overall efficiency of the system.

22. Referring to claim 2, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used (Hung column 9, line 5 to column 10, line 5), the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first function by forming one or more additional instances of the first functional unit (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

23. Referring to claim 3, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used (Hung column 9, line 5 to column 10, line 5), one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

24. Referring to claim 4, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used (Hung column 9, line 5 to column 10, line 5), the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the

plurality of functions other than the second function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

25. Referring to claim 5, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 1 wherein if a third function is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third function (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

26. Referring to claim 6, Gove has taught an adaptive computing integrated circuit, comprising:

a. a plurality of reconfigurable matrices, the plurality of reconfigurable matrices including a plurality of heterogeneous computational units, each heterogeneous computational unit having a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44

to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64),

b. the plurality of heterogeneous computational units coupled to an interconnect network and reconfigurable in response to configuration information (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64); and

c. a matrix interconnection network coupled to the plurality of reconfigurable matrices, the matrix interconnection network operative to reconfigure the plurality of reconfigurable matrices in response to the configuration information for a plurality of operating modes (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

d. wherein a first group of heterogeneous computational units is reconfigurable to form a first functional unit to implement a first operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

e. wherein a second group of heterogeneous computational units is reconfigurable to form a second functional unit to implement a second operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64);

f. wherein while the first functional unit implements the first operating mode, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

27. Gove has not taught reconfiguring the computational units if the second operating mode is not currently used. Hung has taught reconfiguring multiple computation elements to function on different functions based upon need and availability (Hung column 9, line 5 to column 10, line 5). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hung in the device of Gove to reduce idle time of computation elements and minimize mode switching, thereby increasing the overall efficiency of the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the reconfiguring of Hung in the device of Gove to improve overall efficiency of the system.

28. Referring to claim 7, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used (Hung column 9, line 5 to column 10, line 5), the one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode by forming one or more additional instances of the first functional unit (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

29. Referring to claim 8, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used (Hung column 9, line 5 to column 10, line 5), one or more of the first group of heterogeneous computational units and the one or more of the second group of heterogeneous computational units are reconfigurable to form a single functional unit to implement the first operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

30. Referring to claim 9, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used (Hung column 9, line 5 to column 10, line 5), the one or more of the second group of heterogeneous computational units are reconfigurable to implement one or more of the plurality of operating modes other than the second operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26,

line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

31. Referring to claim 10, Gove in view of Hung has taught the adaptive computing integrated circuit of claim 6 wherein if a third operating mode is to be implemented, one or more of the first group of heterogeneous computational units and/or the one or more of the second group of heterogeneous computational units are reconfigurable to implement the third operating mode (Gove column 9, line 27 to column 10, line 4; Figure 10;column 11, lines 23-65; Figure 16; column 15, lines 52-63; Figure 17; column 26, lines 19-34; column 26, line 44 to column 27, line 33; Figure 28; column 61, line 60 to column 62, line 52; Figure 61: Figure 62: Figure 63: Figure 64).

32. Claims 11-20 have similar limitations to claims 1-10 rejected above and are rejected for similar reasons.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Kogge, U.S. Patent Number 5,475,856, has taught a system for dynamically configuring SIMD and MIMD mode operations.

b. Blamer et al., U.S. Patent Number 5,226,125; Ing-Simmons et al., U.S. Patent number 5,239,654; and Gove et al., U.S. Patent Numbers 5,371,896; 5,471,592; 5,522,083; 5,613,146; 5,696,913; 5,768,609; 6,070,003; and 6,260,088 are all related patents to primary reference used in the rejection above.

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183

12 June 2009